

Advanced Fault Detection

Ground Fault and Arc Fault Circuit Interrupters

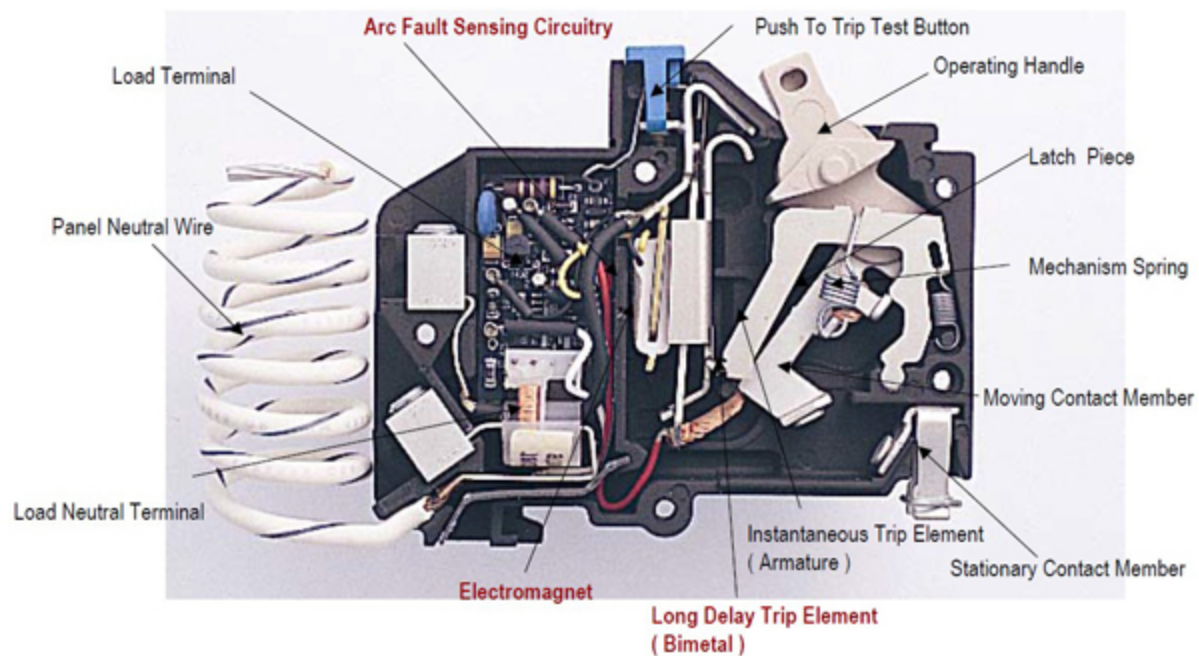


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Introduction

Managing fault currents is a critical aspect of electrical safety. It only takes a few milliamperes of current flowing through a person to kill them in about a second. While devices should be designed to not allow line voltage to be exposed to a human during normal operation or most failures, redundancy, particularly in higher risk environments like wet areas, is desirable (Mullin et al., 2018, p. 178). Circuit breakers provide one level of safety, overcurrent protection on the line itself. If hot and neutral are bridged or if a device draws too much current, the current flow will cause the breaker to trip and cut the connection, protecting the lines themselves from damage, and from heating up enough to start a fire. However, the few milliamperes of current needed to cause electrocution is not enough to trip a breaker rated for 15 amperes, and it may not flow along the conventional current path, instead going to ground by the easiest possible means, what is called a ground fault. This is what ground fault circuit interrupters (GFCIs), also known as residual current devices (RCBs) detect and prevent. Another type of fault is the arc fault, the electric arc caused by a poor connection. While electric arcs are present temporarily during normal operation of many devices, such as switches and motors, or during the process of inserting an electrical plug into an outlet, the heat of hazardous, abnormal arcs can start fires. Arc-fault circuit interrupters (AFCIs) are a way to protect against these, detecting dangerous arcing and cutting the power, while ignoring expected arcs. Electrical codes may require one or both in certain circumstances, such as bedrooms, kitchens, bathrooms, or on outdoor outlets.

Types, Code Requirements, and Installation

The type of protection a GFCI or AFCI provides depends on its location. A GFCI or AFCI installed at the panel (usually as part of a combination breaker/AFCI/GFCI) will protect the entire branch circuit connected to it. If a GFCI or AFCI receptacle is the first in a branch circuit, it will protect all outlets after it in the circuit, if connected as a feed-through. An AFCI receptacle will not protect against parallel arcing upstream of the device, however (Eaton Residential Products Group, 2014). The Canadian Electrical Code requires arc-fault protection on all circuits supplying 125V receptacles rated 20A or less (CEC 2021 Rule 26-658 1), with exceptions for garages, laundry rooms and other areas where

nuisance-tripping would be high or the risk of fire is low. That protection can be supplied either via a combination breaker/AFCI at the panel or via an AFCI receptacle placed as the first outlet in the circuit, if the wiring between the panel and that first receptacle is run within a metal raceway, armoured cable, or non-metallic conduit or tubing (CEC 2021 Rule 26-658 2), all much less likely to allow a fire to catch than non-armoured cable run bare through studs. GFCI receptacles can be used in a similar way, though nuisance-tripping can become a problem on long branch circuits.

Receptacles

GFCI receptacles are mandated by code in wet areas, such as near sinks or outdoors (CEC 2021 Rules 26-704 and 26-720). A GFCI or AFCI outlet is distinguishable from a standard outlet by the two buttons on its face, one to test the outlet, the other to reset it in the event of a fault, and often one or more LEDs, as shown in the image. If LEDs are present, one will show that power is present and the other will illuminate in the event of a fault. GFCI and AFCI receptacles generally look quite similar, with only the text on the front face to specify which functionality the outlet has.



Figure 1: A typical North American residential GFCI outlet, installed (Kurtovic, 2021)

GFCI receptacles are part of the special case in electrical installation where, in the scenario where a non-bonded receptacle is being replaced and bonding is not available at the outlet location (due to the existing wiring being knob-and-tube wiring that lacks a bonding conductor, for example), the bonding terminal of the GFCI outlet and any subsequent bonded receptacles connected down-stream of it is not required to be connected to ground or other outlets, and connecting it is in fact prohibited by the Canadian electrical code (Mullin et al., 2018, p. 187). This is one way in which the electrical code accommodates existing out-of-date wiring and allows its safety and compatibility with modern devices to be improved economically.

At the panel

GFCI or AFCI circuit breakers usually look like any other circuit breaker, with the addition of a test button alongside the standard toggle for the breaker, and often a ground or neutral lead. While it is common since some electrical codes started mandating a level of arc-fault protection, starting with the USC National Electrical Code in 1999 (Lee et al., 2000, p. 160) to put arc-fault protection at the panel, it is less common to put ground-fault protection there, because ground-fault



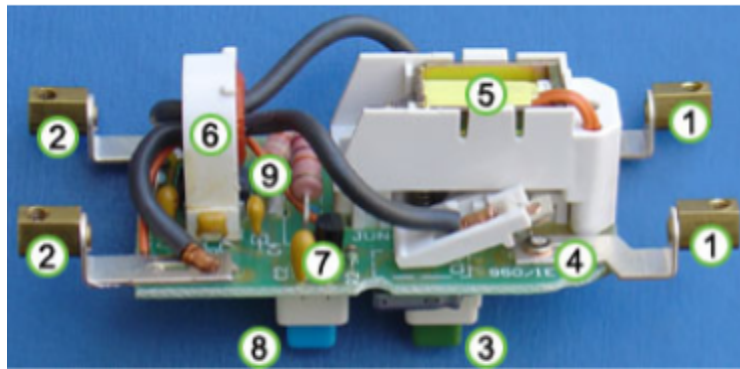
Figure 2: Panel-mount AFCI combo single-pole breaker (Eaton, 2014)

protection is often only required on specific outlets, while arc-fault protection is generally required for an entire branch circuit (since an arc fault anywhere on the circuit can cause heating in more than one location). Also, the rate of nuisance-tripping on ground fault-protected circuits increases dramatically with the number of outlets on the circuit, because the individually small and non-hazardous ground leakage currents add up.

Regulatory differences

Arc-fault protection code requirements are substantially stricter in North America than in Europe and Australia. One can contrast the numerous places they are required by the CEC detailed above with the direction in the equivalent document for Australia and New Zealand, which recommends in an appendix that they be installed “where there is significant risk of electrical fire” (GSES, 2018) and doesn’t mandate them in any location. This is likely due to the greater prevalence of wood-framed construction in North America and the prevalence of non-metallic sheathed cable run unprotected through walls with wood studs (instead of conduit within concrete or brick, as is more typical outside of North America). 230V residential circuits also tend to carry lower currents that arc less dangerously (welding short, thus triggering overcurrent protection, or burning clear, rather than continuing intermittently and causing heating), for the same wattage of load.

Anatomy and Operating principles



1. Incoming terminals
2. Outgoing terminals
3. Reset button
4. Contact
5. Solenoid
6. Sense coil
7. Sense circuitry
8. Test button
9. Test wire

Figure 3: European GFCI anatomy (Ali, 2004)

Arc-fault and ground-fault detecting devices operate on similar principles. They use a pair of coils forming a current transformer placed around the current-carrying conductors to detect current flowing in them. More specifically, they detect a difference in the current flowing in the conductors (the difference usually occurring because said current is flowing to somewhere else). The output of that sense coil is then fed into circuitry that detects any anomalous current flow and triggers the solenoid to move the contact and break the circuit. For ground faults, this must happen quickly to avoid allowing a potentially lethal amount of electricity to flow through the fault source (possibly a person). The exact amount of current and required speed of triggering depends on the electrical code. The CEC requires that a Class A GFCI trip from a 6 mA or greater current to ground, within 4 seconds (though most Class A GFCIs trip in under a second) for that 6 mA current, decreasing to 40 milliseconds (usually 20 ms for actual Class A devices) for 260 mA currents (Mullin et al., 2018, p. 178). For arc faults, the standard is to trip if 8 half cycles of arcing (evidenced by high frequency oscillations, characteristically around 100 KHz) occur within a 0.5 second window (Lee et al., 2000, p. 152). Both types of devices can include additional sensors, such as temperature sensors, to enhance the accuracy of their fault detection. An arc-fault detector, with its generally more advanced circuitry, can also easily detect ground faults, though not all are rated as proper GFCIs.

GFCI operation example: the LM1851

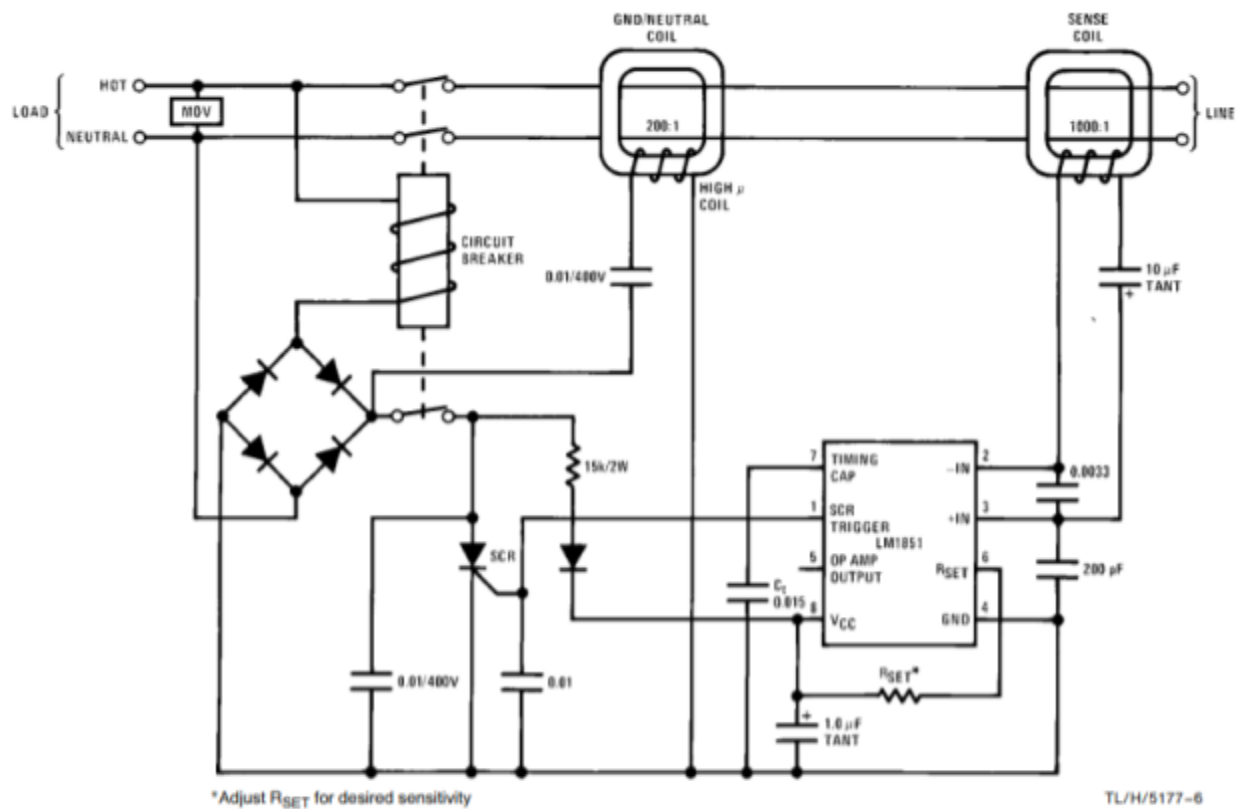


Figure 4: LM1851 Application Circuit (National Semiconductor Corp., 2011)

The LM1851 is an early and common ground-fault detection integrated circuit, present in as many as half of all GFCIs on the market (Sauer, 2004). The schematic, along with a typical application circuit, is available in the datasheet (National Semiconductor Corporation, 2011). It makes a good point of entry for explaining the operating principles. Power is supplied to the IC via a rectifier through a current-limiting resistor, internally regulated to 26 volts. One or two coils are placed on the lines, depending on whether faults in the neutral line must be detected or not. The additional coil in Figure 4 (optional, depending on regulatory requirements) is driven with 120 Hz pulses off of the rectifier output, and some of that energy couples into the sense transformer if the neutral has a ground fault, allowing the GFCI to sense that condition. The sense coil forms a transformer with a 1000:1 turns ratio which is connected through a capacitor to the inputs of the IC (the inverting and non-inverting inputs of an op-amp). When a fault current is present, this induces a current at the inputs, which affects the charging and discharging cycle of the timing capacitor. The

imbalance means the timing capacitor starts holding a charge, and when it reaches the threshold voltage of 17.5 V, it engages a latch and turns off a transistor, allowing current to drive the gate of the SCR which in turn actuates the circuit breaker and cuts the power.

Settings and timing example

A resistor sets the fault current and the value of the timing capacitor determines how fast the device trips. The value of the set resistor is determined by the following equation:

$$R_{SET} = \frac{7V}{I_{f(rms)} \times 0.91}$$

This gives a value of 1.5MΩ for the set resistor if the fault current

threshold is to be 5 mA rms. The timing capacitor value is determined by the equation

$$C_t = \frac{I \times T}{V}$$

where T is the integration time, V is the threshold voltage, and I is the average

fault current into C_t . The UL specification used by the NEC and CEC requires an average trip time under 25 ms. The integration time starts with that value, minus 3 ms GFI turn on time, minus 8 ms due to the possible loss of a half cycle because of how the fault current is sensed, minus 4 ms to open the circuit breaker in the worst case, which leaves 10 ms. T is then selected to be 8 ms for a safety margin and to accommodate deviations in component values within their tolerance, and other potential variables. A worst-case timing

scenario for I (a simultaneous heavy normal fault and a ground fault, during start-up of the IC) is calculated as in Figure 5. R_B is the effective impedance of the short of a normal fault through the human body. R_N and R_G represent the impedance of the circuitry shunting some portion of the fault current around the GFI (particularly in the configuration that accommodates neutral faults). This results in a calculated required C_t value of 0.01μF. However, too low a capacitance increases noise sensitivity and the risk of nuisance tripping. The manufacturer ends up recommending a somewhat higher timing capacitor value of 0.015μF as a compromise. Newer ICs obviously perform better.

$$I = \underbrace{\left(\frac{120 \text{ V}_{AC(rms)}}{R_B} \right)}_{\text{heavy fault current generated (swamps } I_{TH})} \times \underbrace{\left(\frac{R_N}{R_G + R_N} \right)}_{\text{portion of fault current shunted around GFI}} \times \underbrace{\left(\frac{1 \text{ turn}}{1000 \text{ turns}} \right)}_{\text{current division of input sense transformer}} \times \underbrace{\left(\frac{1}{2} \right)}_{C_t \text{ charging on half-cycles only}} \times \underbrace{(0.91)}_{\text{rms to average conversion}}$$

Figure 5: Fault current input for LM1851 GFI (National Semiconductor Corp., 2011)

Reliability, fault current thresholds, and testing

One of the challenges in fault detection is avoiding nuisance tripping. Nuisance trips are not just annoying, they also mean that users are less likely to trust the device when it trips correctly and less likely to notice if the device is faulty. This was also an issue with early arc-fault circuit breakers. People didn't like them and electricians tended to avoid installing them where they could because they were substantially more costly, given the electronics inside, and sometimes tripped for no reason, necessitating the user go to their breaker panel and reset it, or find the outlet and reset it.

The GFCI needs to trip fast enough at a low enough current to protect a person, but also must not trigger in conditions which aren't dangerous. For example, a noisy inductive load like a mixer (a device often present in kitchens where GFCI outlets are required around the sink) could cause a temporary difference in current between the lines due to the inductance of the motor causing the current to lag behind the voltage which might be read instantaneously as a fault. Thus, a relationship between the fault current and needed trip time was established (Figure 6), so that borderline fault

currents could take longer than $\frac{1}{2}$ a 60 Hz cycle to trip (enough that the timing capacitor in the above circuit would get refilled, up to 5 seconds) but higher, dangerous fault currents would still cause a fast trip (Sauer, 2004).

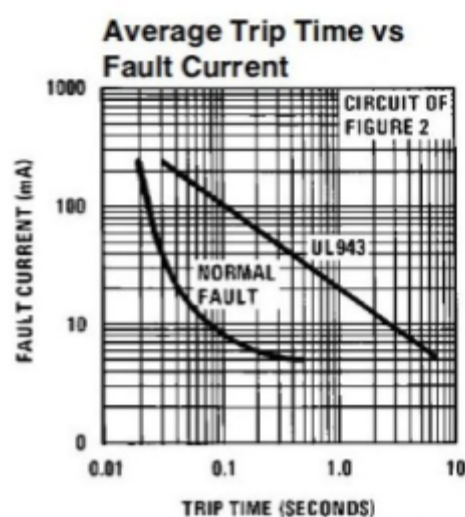


Figure 6: current/time relationship (National Semiconductor, 2011)

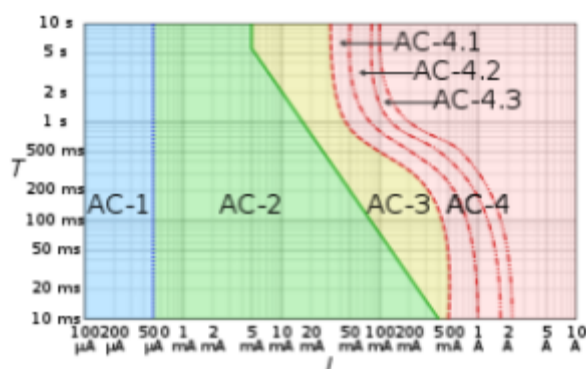


Figure 7: Body current passing thresholds (Wikimedia Commons, 2014)

The fault current threshold was determined based on experimental data. Currents in the AC-3 range in Figure 7, highlighted in yellow, cause a muscle reaction but no permanent effects. Above AC-4.1, there is a nontrivial chance of causing fibrillation in the heart, and above AC-4.3, the chance is above 50%.

Currents above 10 mA can cause uncontrollable muscle contractions and leave the victim unable to voluntarily release an electrified object (Cadick et al., 2005, pp. 1–4). That 10mA threshold marks the true beginning of the danger zone, because it vastly increases the time the victim of an electrical injury is exposed to the current, absent intervention. Standards organisations set the threshold at 5mA for GFCIs intended to protect people (vs equipment) to accommodate infants, the elderly, and others more vulnerable than the average college student used in most tests (Sauer, 2004). The need for a faster trip comes from the fact that if even 6 μ A is delivered to the heart muscles at the wrong point in its contraction cycle it can cause ventricular fibrillation. Interrupting the circuit as quickly as possible reduces this likelihood.

Arc Fault Detection

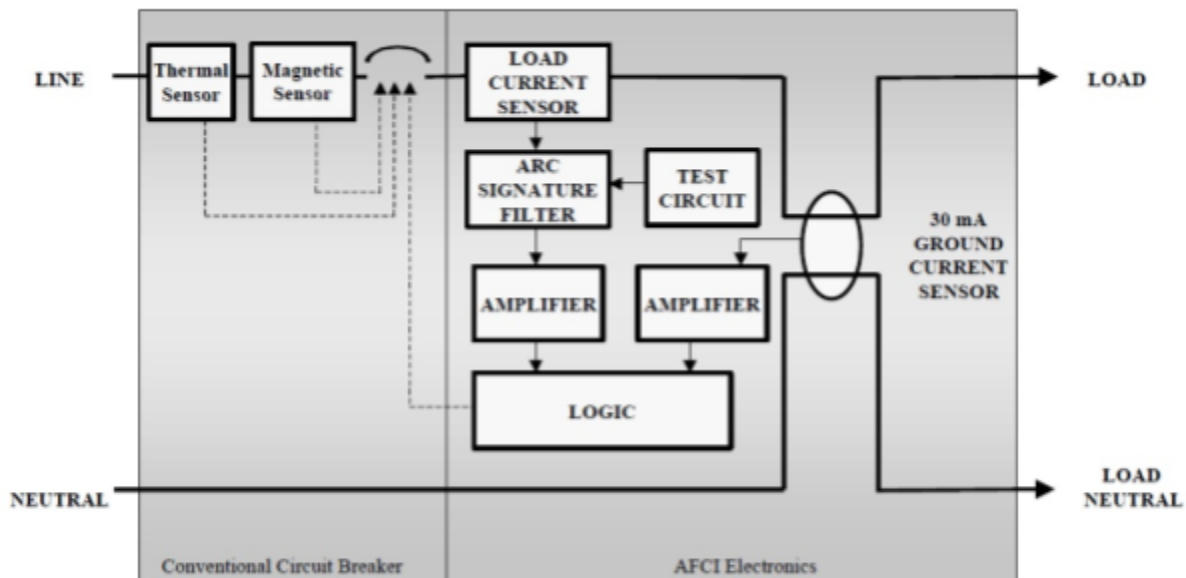


Figure 8: AFI Block diagram (Lee et al., 2000, pp. 152)

Detecting arc faults is also very much a game of sensing the currents quickly and accurately without false positives that cause nuisance tripping. Arc faults add impedance to the circuit and reduce the current flow. Parallel arcing has an even greater effect, because the erratic current flow reduces the RMS current which is what a standard circuit breaker effectively measures. Furthermore, there are good and bad arcs, as previously discussed. “Good” arcs are periodic and repetitive on the normal cycle (60 Hz) and are often non-sinusoidal (Lee et

al., 2000, pp. 151–152). Bad arcs are nonperiodic, or non-repetitive, their frequency differs substantially from the line frequency.

The arc signature filter can be analog and feed into application-specific logic circuits, or it can be done using digital signal processing on a microprocessor. A ground current sensor (seen in Figure 8) can also feed into the logic, allowing it to detect slowly-developing problems that tend to precede arc faults, as well as ground faults. Thus, the logic can be more sensitive if preconditions are present and less sensitive if they are not, reducing the chance that the device triggers in the absence of a hazardous fault.

Sample Arc fault detection hardware

A Texas Instruments evaluation board for arc detection in photovoltaic circuits (Texas Instruments, 2023) can serve as an example. This circuit is intended for DC arc detection, but the same principles apply to AC, there is just the additional 60 Hz signal to filter out, thresholds for detection must be set higher. It analyses the 30 kHz to 100 kHz frequency band. The frequency range imposes certain requirements on the analog-digital converter used, because the sampling frequency of the ADC must be equal to or greater than twice the Nyquist frequency, the maximum frequency analysed, to prevent aliasing and associated errors (Leis, 2011, p. 82). The input of the device is a current transformer with the following schematic:

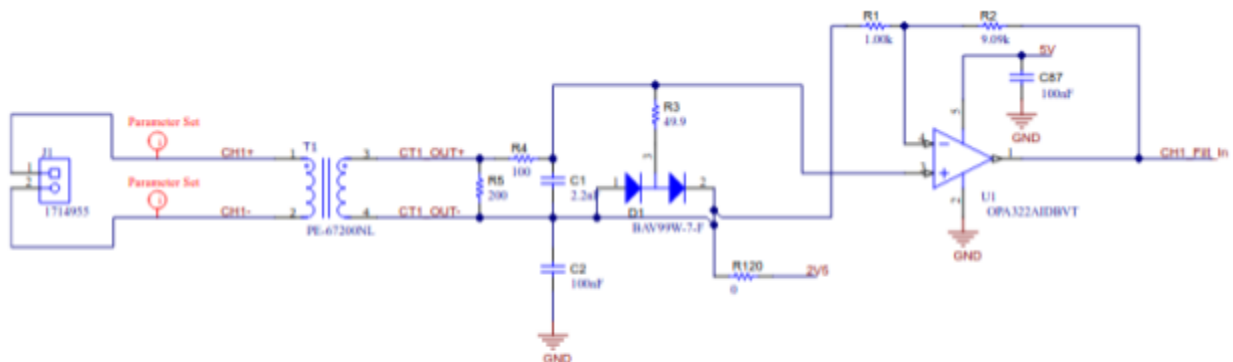


Figure 9: Current transformer and gain stage (Texas Instruments, 2023)

This converts the AC components of the current into a voltage using the burden resistor R5, then amplifies it ten times to fit it into the voltage range of the filter stage and biases it.

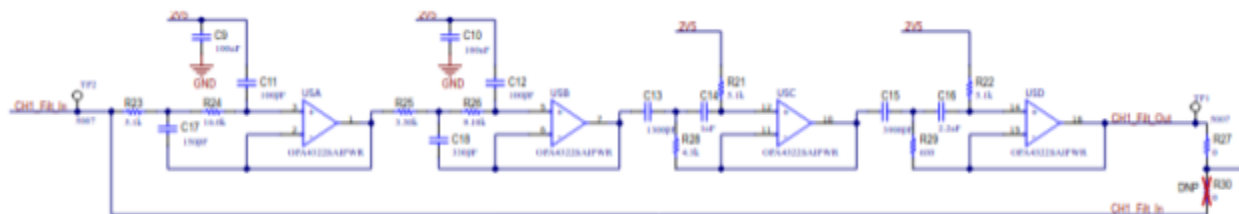


Figure 10: Filtering stage, band-pass filter, 30 kHz to 100 kHz (Texas Instruments, 2023)

The filter has a gain of 1 in the pass band, dropping off within one order of magnitude on either side to -50 dB. Selection of the op-amp used for filtering primarily depends on its frequency response within the relevant bandwidth.

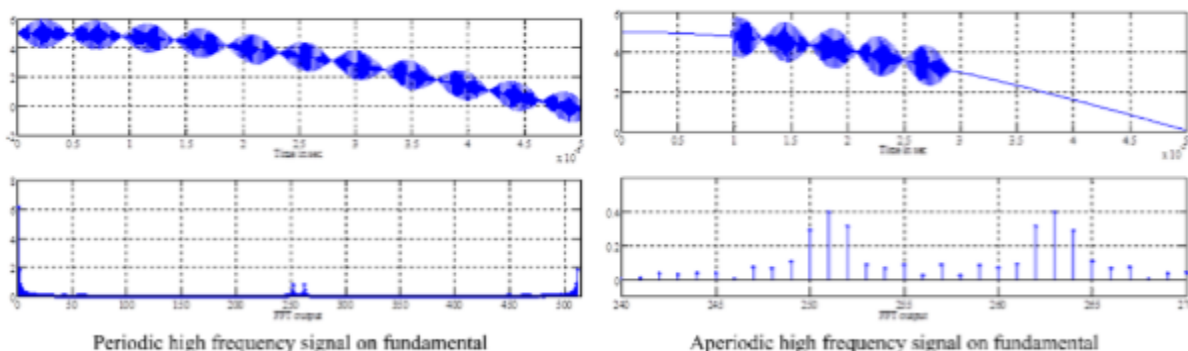
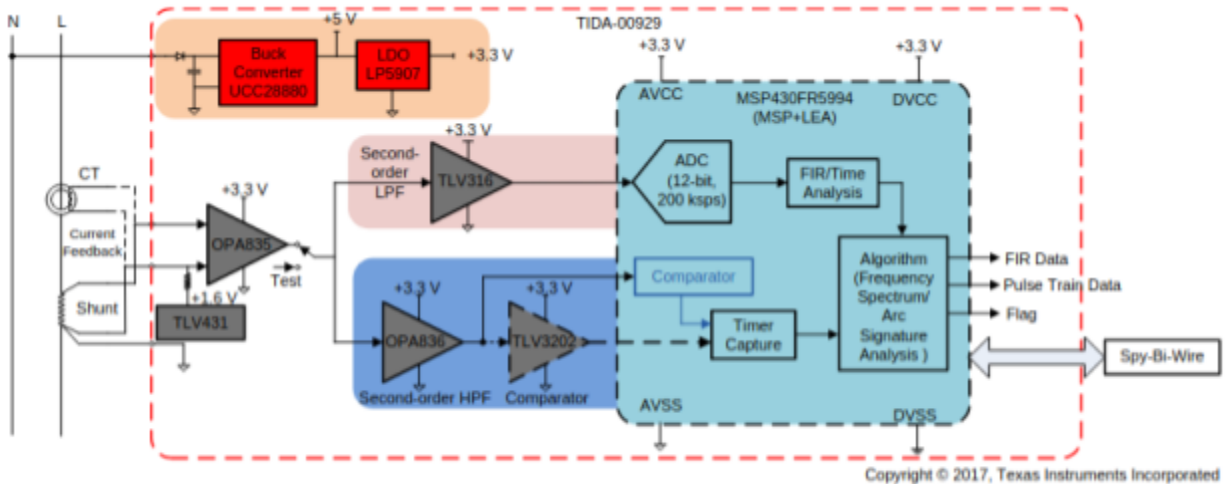


Figure 11: FFT analysis of periodic & aperiodic noise (Texas Instruments, 2019)

The arc detection here is based on frequency domain analysis using the fast Fourier transform, a very common signal processing method (Figure 11). The noise of the arc itself has quite a wide distribution, up to several megahertz, but because of cable geometry, the density of the noise currents above 200kHz vary significantly with the frequency. Below 100 kHz is more consistent. 10 kHz is the floor. However, circuits like inverters and switching power supplies which may be connected to the power lines and serve as noise sources operate in this band, and so the exact band monitored must be tuned to avoid them (Texas Instruments, 2023, p. 12). The detection algorithm performs a FFT on the sampled signal and sums up the noise in the specified frequency band. The output can then be weighted toward a particular frequency, thresholds set, and conditions for discarding spurious peaks in the signal specified. If a lot of noise occurs only in one or a few isolated samples, then it isn't an arc, an arc will appear more consistently in the time domain, even if very intermittent, because of the high sample rate. Tuning these parameters correctly can produce a detection rate which satisfies regulatory standards.

Transients and response speed



Another TI reference design, depicted in Figure 12, demonstrates additional capabilities relevant to actual AFCI applications. This circuit implements two parallel analog signal paths through which the current transformer output passes after going through initial amplification and biasing. One goes through a low-pass filter stage (to reduce aliasing issues by eliminating the high frequency components of the input) and into the ADC of the MCU, similar to the previous circuit. The other is sent through a high-pass filter (in actuality a band-pass filter, because the chosen op-amp's frequency response imposes an upper bound on what it will pass) and either tapped off there and taken into a comparator in the MCU, or sent through an analog op-amp comparator and into the MCU's digital inputs. In reality, many AFCIs will use only one of these, with cheaper devices perhaps using the simpler, less demanding, but less accurate comparator pathway. The advantage to the comparator pathway, however, is speed. An ADC has a limited sample rate and processing time relative to the clock speed of most MCUs. A comparator on a microcontroller pin is virtually instant by comparison, and can be captured at a consistent rapid rate with very low compute usage using a hardware timer. The comparator output can be used to detect transient faults, not just persistent ones. If both pathways are present, the comparator can be used to activate the MCU for measurement and quick fault response while leaving it asleep the rest of the time (Texas Instruments, 2019, pp.3-4).

Conclusion

Fault currents that do not involve short circuits can prove difficult to detect. Ground faults can be handled with an IC containing a moderate number of transistors, but the frequency analysis needed to reliably detect arc faults usually demands a general-purpose MCU in practice. While very economical MCUs, op-amps, and other chips are on the market, the need for residential arc fault protection in particular still imposes something of a cost on homeowners and developers. The difference in needs between continents is remarkable, given that it is largely down to chance or historical contingency that particular voltages were chosen for common residential use, which in turn affected the rate of hazardous arc fault conditions. Typical circuit breakers in Europe, due to the lack of AFCI protection requirements, are on average much, much simpler, often containing little more than bimetallic strips and metal oxide varistors.

Ground fault protection is a much more generally applicable safety measure. Arc-fault detection and protection, which in practice ends up being something of a superset of the previous, given that most arc fault detectors can also detect ground faults, veers quickly into physics, analog analysis, and algorithm design, which this paper has only scratched the surface of.

Distinguishing proper electrical behaviour from the merely odd and from the dangerous and responding accordingly is an ongoing challenge, made more so by other historical architectural and regulatory choices.

References

- Ali & Wikimedia Commons. (2004). *photo of electrical Residual-Current Circuit Breaker*.
<https://en.wikipedia.org/wiki/File:ResidualCurrentCircuitBreak.jpg>
- Cadick, J., Capelli-Schellpfeffer, M., & Neitzel, D. (2005). *Electrical safety handbook 3E*. McGraw Hill Professional.
- Canadian Standards Association. (2021). *Canadian electrical code. Part 1: Safety standard for electrical installations*. (25th edition). CSA Group.
- Eaton Residential Products Group. (2014). Understanding the 2015 Canadian Electrical Code Requirements for Arc-Fault Protection. In *White Paper WP003001EN*. Eaton Canada.
<https://www.eaton.com/content/dam/eaton/products/electrical-circuit-protection/circuit-breakers/residential-circuit-breakers/2015-Canadian-Electrical-Code-Requirements-for-Arc-Fault-Protection.pdf>
- GSES. (2018, July 24). *Wiring rules AS NZS 3000:2018 – key updates to the standard and what they mean for installers*. GSES. <https://www.gses.com.au/wiringrulesasnz3000/>
- Kurtovic, B. & Wikimedia Commons. (2021). *Residential GFCI receptacle*.
https://en.wikipedia.org/wiki/File:Residential_GFCI_receptacle.jpg
- Lee, D. A., Trotta, A. M., & King, Jr., W. H. (2000). New technology for preventing residential electrical fires: Arc-fault circuit interrupters (AFCIs). *Fire Technology*, 36(3), 145–162.
<https://doi.org/10.1023/a:1015410726786>
- Leis, J. W. (2011). *Digital signal processing using MATLAB for students and researchers*. John Wiley & Sons.
- Mullin, R. C., Branch, T., Gerolimon, S. F., Simmons, J. P., & Trineer, C. (2018). *Electrical wiring: Residential*. Nelson Education.
- National Semiconductor Corporation. (2011). LM1851 ground fault interrupter. In *Digikey Datasheets*. Texas Instruments, Incorporated.

<https://media.digikey.com/pdf/Data%20Sheets/Texas%20Instruments%20PDFs/LM1851.pdf>

Sauer, D. (2004). *Ground Fault Interrupters*. Idea2IC.Com.
<http://www.idea2ic.com/GFI/GFICs.html>

Shekhar, A., Ramirez-Elizondo, L., Bandyopadhyay, S., & Bauer, P. (2017, May 23). *Detection of series arcs using load side voltage drop for protection of low voltage DC systems*. IEEE (Institute of Electrical and Electronics Engineers).
https://www.researchgate.net/publication/317106136_Detection_of_Series_Arcs_Using_Load_Side_Voltage_Drop_for_Protection_of_Low_Voltage_DC_Systems

Texas Instruments. (2019). Spectrum analyzer: Signal conditioning/processing for capturing arc ref design (rev. E). In *Design Guide: TIDA-00929*. Texas Instruments, Incorporated.
<https://www.ti.com/lit/ug/tiducg7e/tiducg7e.pdf>

Texas Instruments. (2023). Analog front end for arc detection in photovoltaic applications reference design (rev. B). In *Design Guide: TIDA-010321*. Texas Instruments Incorporated. <https://www.ti.com/lit/ug/tiduez9b/tiduez9b.pdf>

Wikimedia Commons. (2014). *Log-log graph of the effect of alternating current I of duration T passing from left hand to feet as defined in IEC publication 60479-1, redrawn based on Weineng Wang, Zhiqiang Wang, Xiao Peng, "Effects of the Earth Current Frequency and Distortion on Residual Current Devices", Scientific Journal of Control Engineering, Dec 2013, Vol 3 Issue 6 pp 417-422. .*
https://en.wikipedia.org/wiki/File:IEC_TS_60479-1_electric_shock_graph.svg